

FIG. 1

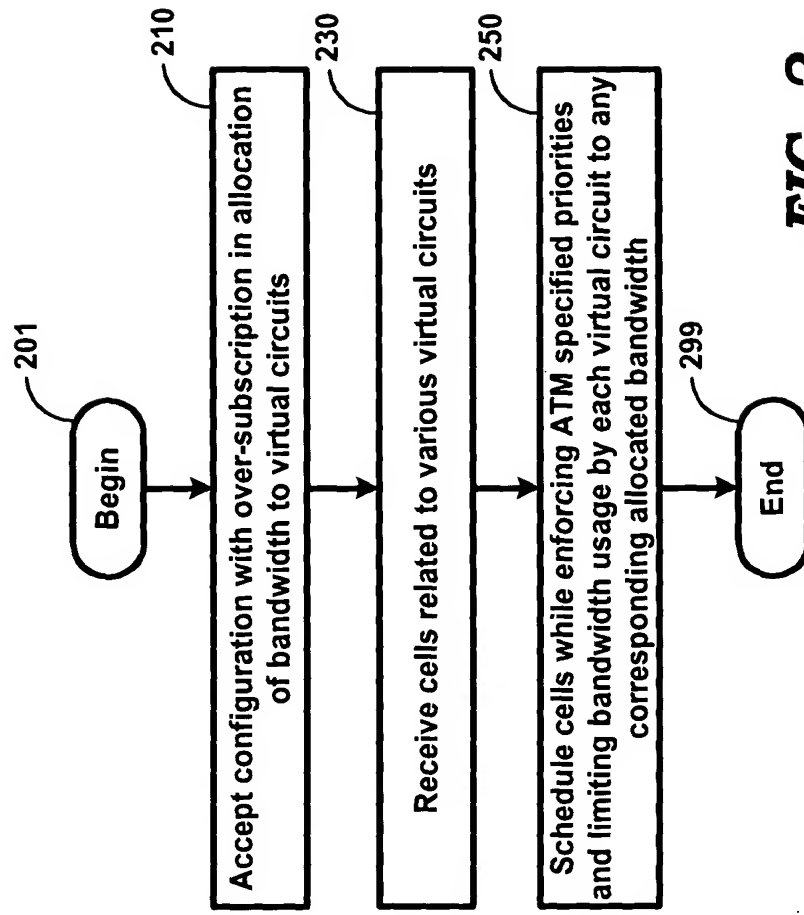


FIG. 2

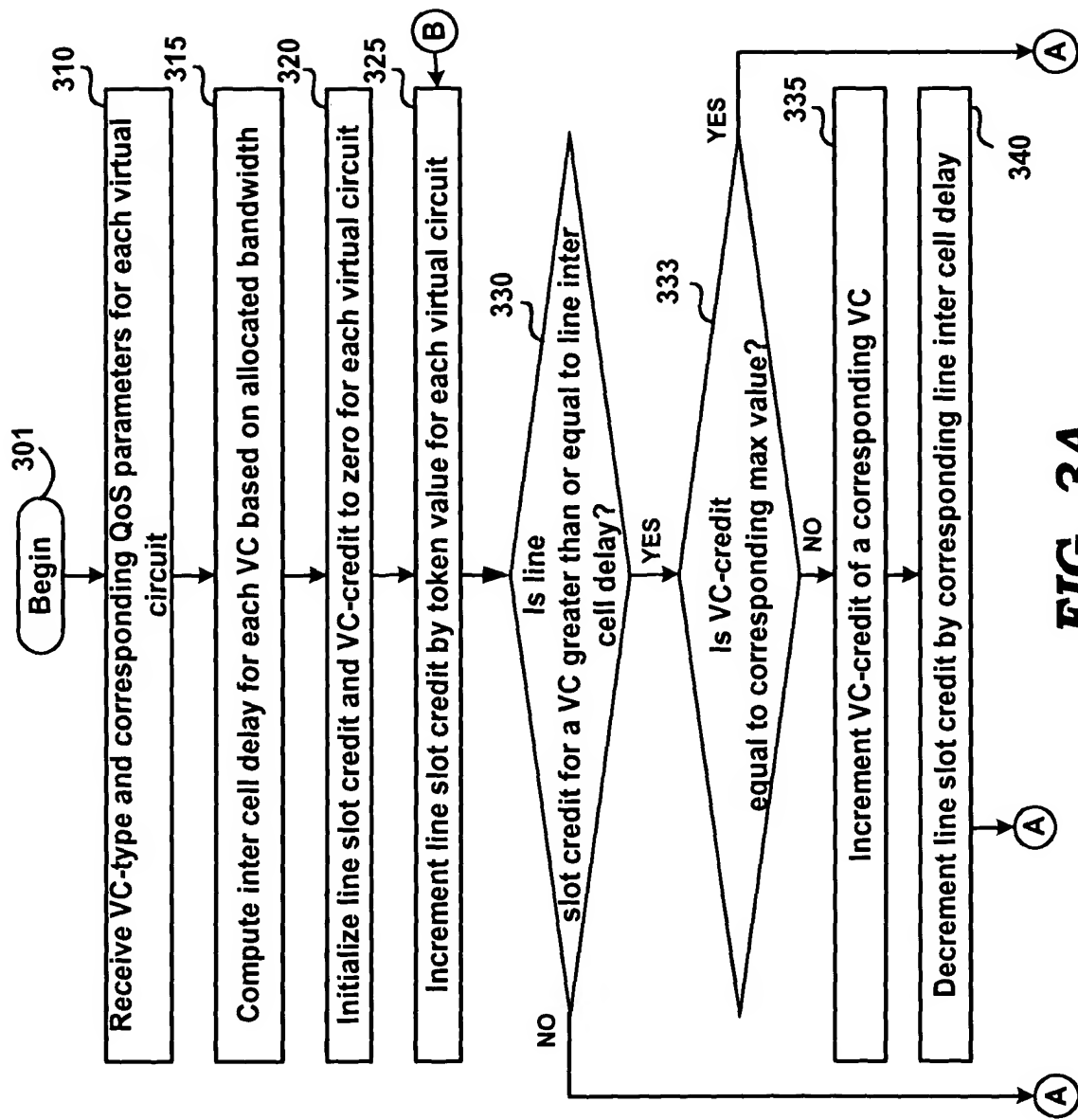
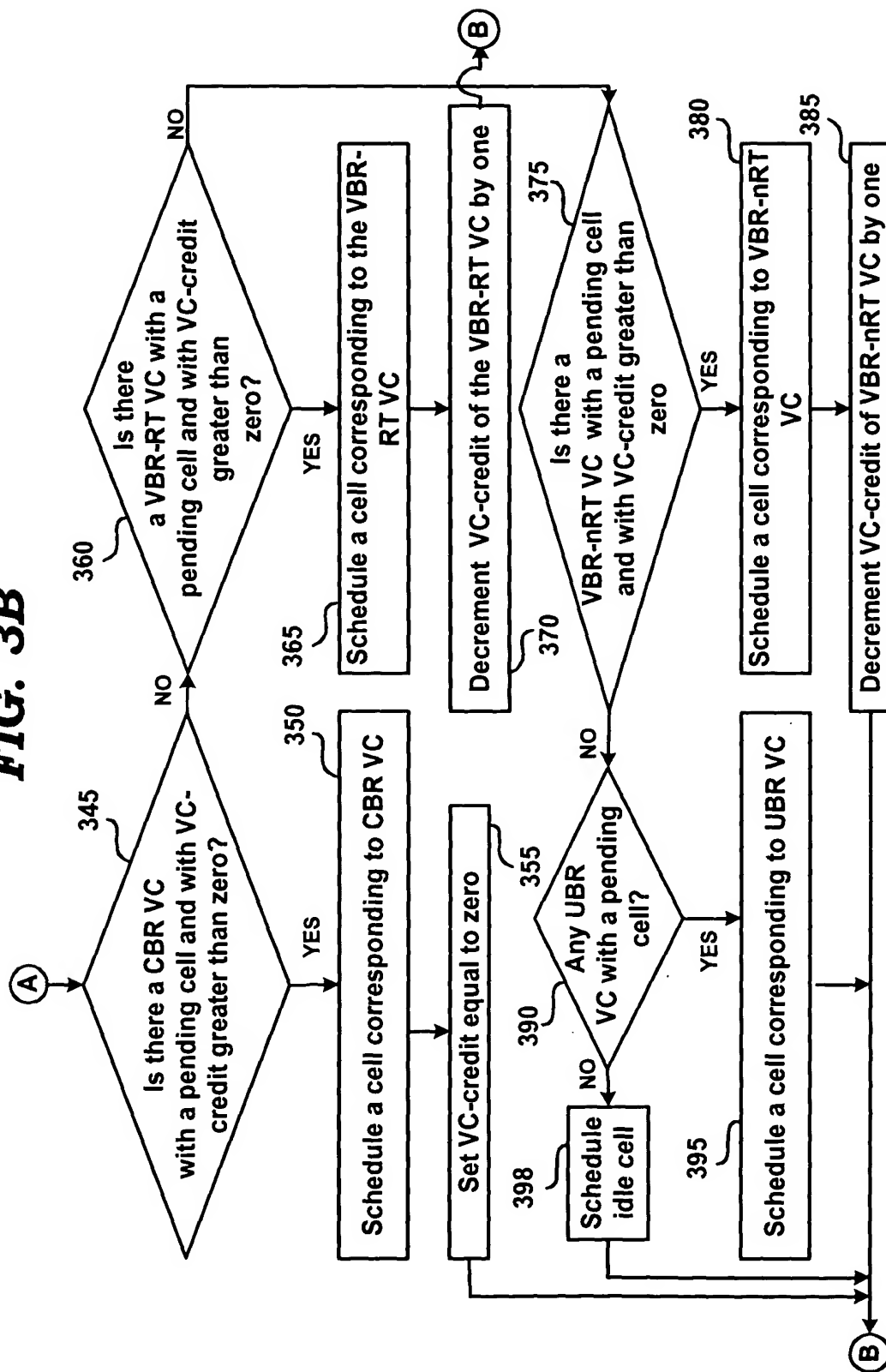


FIG. 3A

FIG. 3B



	401	402	403	404	405	406	407	408
Line_Slot_Credit	100	200	100	200	100	200	100	200
Cell Slot	0	VC1	0	VC1	0	VC1	0	VC1
Line_Slot_balance	100	0	100	0	100	0	100	0
Cell Spacing	idle	VC1	idle	VC1	idle	VC1	idle	VC1
Transmitted Cell	idle	idle	idle	idle	idle	idle	idle	idle
VC-Credit	0	1	1	2	2	3	3	3

FIG. 4A

Line_Slot_Credit	100	200	175	150	125	100	200	175	150	125	461
Cell Slot	0	CBR	CBR	CBR	CBR	0	CBR	CBR	CBR	CBR	462
Line_Slot_balance	100	75	50	25	0	100	75	50	25	0	463
Line_Slot_Credit	100	200	100	200	100	200	100	200	100	200	464
Cell Slot	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	465
Line_Slot_balance	100	0	100	0	100	0	100	0	100	0	466
Cell Spacing	idle	CBR / VBR -nRT	CBR	CBR / VBR -nRT	CBR	VBR -nRT	CBR	CBR / VBR -nRT	CBR	CBR / VBR -nRT	467
Transmitted Cell	idle	CBR	CBR	CBR	VBR -nRT	VBR -nRT	VBR -nRT	VBR -nRT	idle	VBR -nRT	468
VC-Credit (CBR)	0	0	0	0	1	1	1	1	1	1	469-A
VC-Credit (VBR-nRT)	0	0+1 - 0=1	1+0 - 0=1	1+1 - 0=2	2+0 - 1=1	1+1 - 1=1	1+0 - 1=0	0+1 - 1=0	0+0 - 0=0	0+1 - 1=0	469-B

FIG. 4B

Line_Slot_Credit	100	200	175	150	125	100	200	175	150	125	481
Cell Slot	0	CBR	CBR	CBR	CBR	0	CBR	CBR	CBR	CBR	482
Line_Slot_balance	100	75	50	25	0	100	75	50	25	0	483
Line_Slot_Credit	100	200	100	200	100	200	100	200	100	200	484
Cell Slot	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	0	VBR -nRT	485
Line_Slot_balance	100	0	100	0	100	0	100	0	100	0	486
Cell Spacing	idle	CBR / VBR -nRT	CBR	CBR / VBR -nRT	CBR	VBR -nRT	CBR	CBR / VBR -nRT	CBR	CBR / VBR -nRT	487
Peak_Slot_credit	100	200	200	200	200	158	116	200	158	116	488
Transmitted Cell	idle	CBR	CBR	CBR	VBR -nRT	VBR -nRT	Idle	VBR -nrt	VBR -nRT	Idle	489
Peak_Slot_balance	100	200	200	200	58	16	116	58	16	116	490
VC-Credit (VBR-nRT)	0	0+1- 0=1	1+0- 0=1	1+1- 0=2	2+0- 1=1	1+1- 1=1	1+0- 0=1	1+1- 1=1	1+0- 1=0	0+1- 0=1	491

FIG. 4C

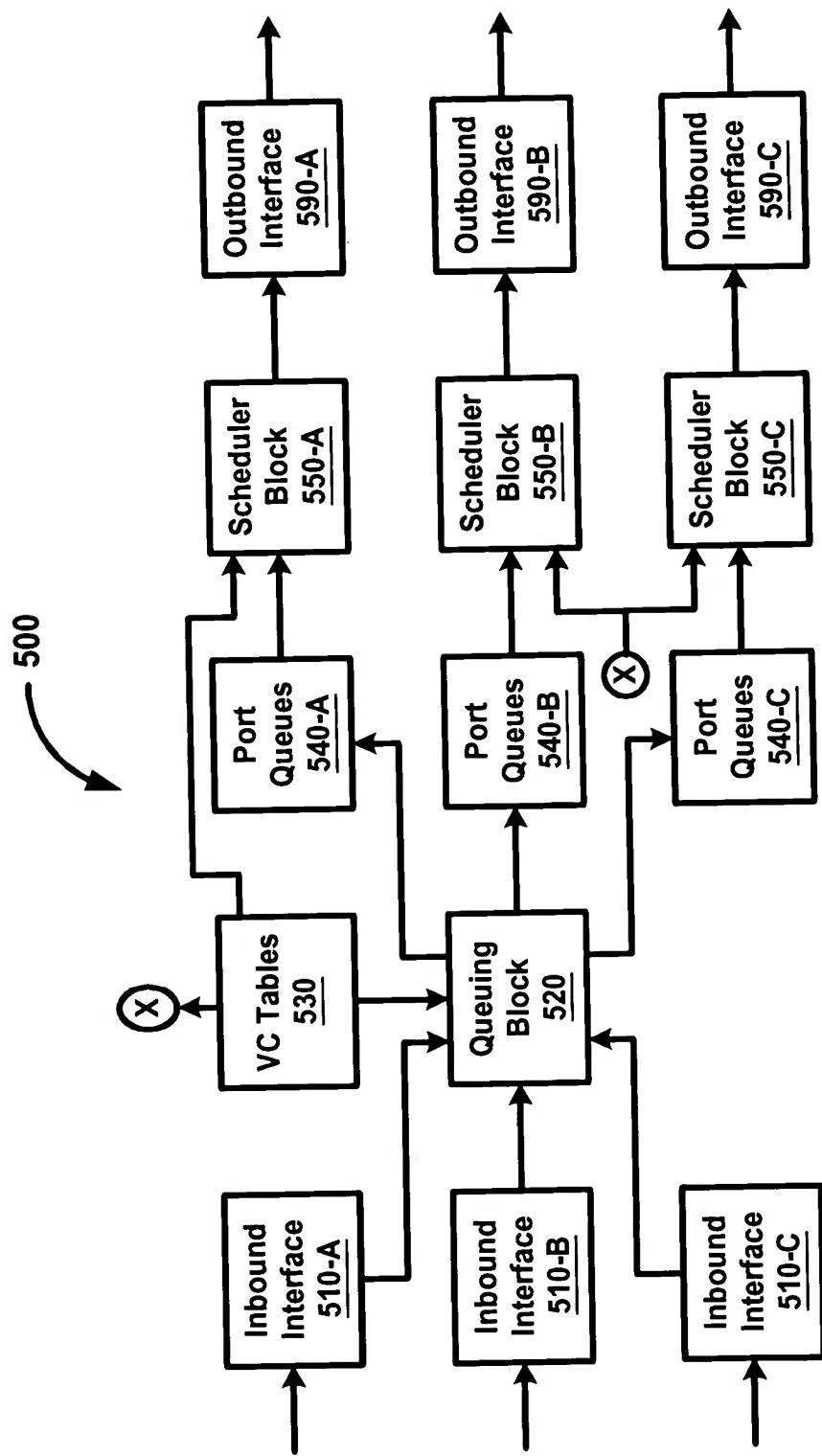


FIG. 5

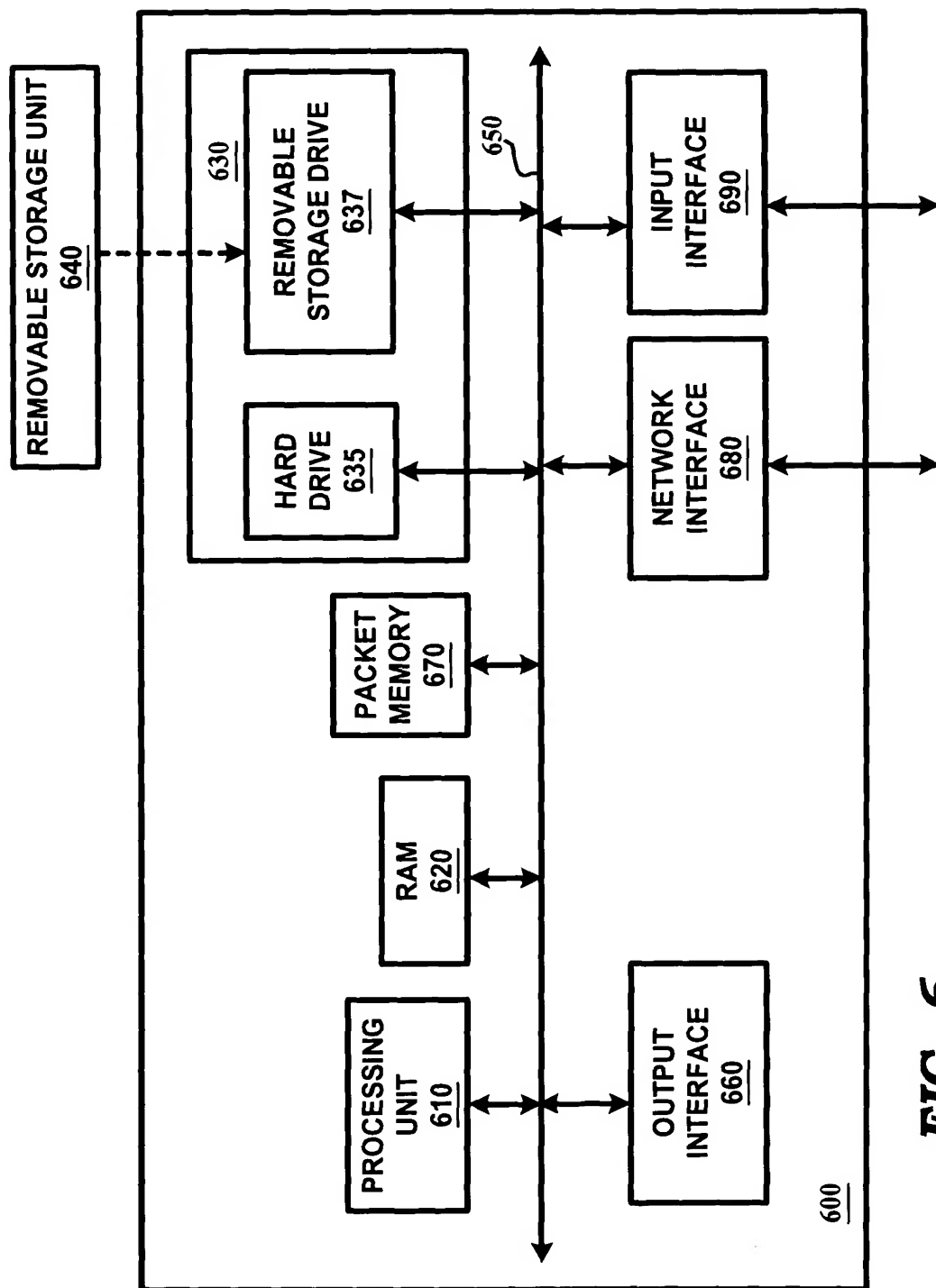


FIG. 6